A 0.5μm Pixel Frame-Transfer CCD Image Sensor in 110nm CMOS

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Abstract

The first image sensor with submicron pixel pitch is reported. Test structures comprising 16 × 16 pixel Full-Frame-Transfer (FFT) CCDs with 0.5μm pixels are fabricated in a single-poly 110nm CMOS process. Characterization results demonstrate charge transfer efficiency of 99.9%, QE of 48% at 550nm, conversion gain of 193μV/e-, well capacity of 3550e-, dark current of 50e-/sec with nonuniformity of 25%, peak SNR of 28dB and dynamic range of 60dB. These performance metrics are within the range of consumer image sensors and suggest that further reduction in pixel size is feasible.

Introduction

Pixel scaling in image sensors has aimed at increasing spatial resolution for a given optical format. As pixel size is approaching the limits of conventional optics, the improvement in resolution is diminishing. Scaling pixels beyond these limits, however, can provide new imaging capabilities beyond merely attempting to increase resolution. In [1], we show that a multi-aperture image sensor comprising a 2D array of apertures, each having its own optics and small submicron-pixel image sensor, can simultaneously capture both a 2D image and a depth map of the scene. We further argue that depth resolution improves with pixel scaling. The general idea is as follows. Each feature in the scene is captured by several apertures. Changing the depth of a feature causes displacements in their positions within the apertures. Depth can then be inferred from these displacements. As discussed in [1], displacements can be measured at higher resolution than the typical spot-size limit of the objective lens. Deeply scaled pixels can also enable high resolution near-field imaging for such applications as microscopy and in vivo imaging [2].

This paper presents the design and characterization of the first submicron pixel image sensor. The reported 0.5μm pixel pitch is 3 times smaller than recently published CCD and CMOS image sensors [3], [4]. To characterize our design, we fabricated test structures comprising arrays of 16 × 16, 0.5μm pixel Full-Frame-Transfer (FFT) CCDs, each with source follower readout circuit, in 110nm single-poly CMOS. We first discuss the design, fabrication, and operation of the image sensor, and then present simulation and characterization results of the test structures.

Design, Fabrication, and Operation

We choose an FFT-CCD architecture to achieve both high optical coverage and large well capacity for deeply scaled pixels and implement the image sensor in CMOS to enable fast multi-aperture sensor readout and the integration of analog and digital circuits. The FFT-CCD image sensor consists of a CCD pixel array, a CCD storage array, a horizontal CCD, and a source follower readout circuit (see Fig. 1). The pixel array uses no metal layers to achieve maximum light sensitivity, while the rest of the image sensor is light shielded by several metal layers that are also used to distribute global control signals.

The image sensor is designed and fabricated in a 110nm CMOS Image Sensor (CIS) process. Fig. 2 shows an SEM of the image sensor. Fig. 3 shows a 4×4 section of the pixel array and Fig. 4 shows SEM cross-sections in both directions. Each pixel consists of a single poly electrode, a channel, and a channel stop. The poly is N+ pattern doped with the S/D implant masked out in between electrodes. No silicide is used in the pixel array area. STI is used as a channel stop in the vertical direction. An SEM of the horizontal CCD with the fill-and-spill input, the floating diffusion for charge to voltage conversion, and the reset gate are shown in Fig. 7. The reset gate is N+ doped with channel implant for negative threshold voltage.

The FFT-CCD performs snap shot imaging using global electronic shutter. The capture of a frame can occur simultaneously with the read out of a previous frame. To minimize pixel pitch, ripple transfer operation (as opposed to the more common phased transfer) is used. An image can be captured by integrating photocharge under each electrode or under every other electrode for interlaced operation. In either case, integration begins by depleting the CCDs of charge via transfer to the upper diffusion V0. During integration, the pixel array electrodes are held at an intermediate voltage V_{store}. At the end of integration, the accumulated charge is ripple transferred row-by-row to the storage array (see Fig. 5). The electrodes between the row of pixels to be read and their storage row are first set to a high voltage V_{transfer} and then the charge is shifted down one row at a time by sequentially applying a negative voltage V_{isolate} to each electrode.

After transferring the charge from the pixel array to the frame buffer, the transfer through the horizontal CCD is performed in even and odd phases. While the even columns are loaded into the horizontal CCD, it is essential to preserve the charge in the odd columns. A simulation of this process is shown in Fig. 6. The charge in the columns under V34 is shifted to V35 (steps 1 and 2 in the figure). The horizontal electrodes are initially held at V_{isolate} to keep all charge under V35. Then, the even horizontal electrodes are brought to V_{transfer}, which forces the even column charge to drain into the horizontal CCD (step 3). Potential barriers between the even horizontal electrodes are enforced by holding the odd

1-4244-0439-X/07/$25.00 © 2007 IEEE

electrodes at V_{isolate}, while the STI region under the horizontal electrodes (shown in the figure) provides the isolation along the horizontal axis. Next, V34 is brought to V_{store} and a partial transfer occurs at the odd columns from V35 to V34 (step 4). A full charge transfer is now forced in both directions by slowly dropping V35 to V_{isolate} (step 5). This transfer mechanism relies on the condition that the fringing field from horizontal electrodes remain larger than that from V34. This condition is satisfied by bringing V34 up to V_{store} at the same time that V35 is dropping to V_{isolate}. Once charge is completely transfered to the horizontal CCD, V34 is set close to V_{transfer} to ensure that all odd column charge is efficiently passed backwards (step 6). Next, each charge in the horizontal CCD is ripple shifted to the floating diffusion node where it is buffered and double sampled using a source follower circuit. This procedure is repeated for the remaining charge in the odd columns confined by the V34 electrode.

Simulation and Measurement Results

Simulated surface potentials along the channel under various conditions are shown in Fig. 8. Applying V_{store} = 0.5V creates potential barriers of 0.3V between electrodes, which facilitates charge confinement under each electrode. During charge transfer, these barriers are overcome by applying V_{transfer} = 1.5V to the receiving electrode and V_{isolate} = -0.5V to the electrode with charge. While these barriers provide single electrode confinement, the well capacity is limited to less than 500e- before smear. Operation of the array using even and odd fields with V_{isolate} applied between the even/odd electrodes during integration increases the well capacity by nearly 10 fold. As such, this two-field approach is used in all reported measurements. We also simulated the amount of cross-talk between neighboring pixels due to drift and diffusion in the bulk by inducing 500e-h pairs in the bulk with transient analysis. Fig. 9 plots the electron density under electrodes for charge induced at 0.5μm and 2.0μm, resulting in 85% and 20% collection at the intended center electrode, respectively. These results show the need to improve cross-talk at longer wavelengths.

Electrical characterization is performed by loading charge patterns into the horizontal shift register through VP. The conversion gain is obtained by measuring the variance of dark shot noise on the floating diffusion. Charge transfer efficiency (CTE) is measured by moving charge packets through all the columns of the vertical array via the horizontal CCD. Noise from the fill-and-spill operation is removed by averaging and the total transfer times are kept short to eliminate corruption from dark current. Fig. 10 plots measured charge versus the number of transfers, which shows CTE of 99.9%. The results of optical characterization are given in Fig. 11-12. Note that despite the use of poly electrodes, the blue response is quite acceptable. This is due to the thin the poly layer and the open space in between each electrode. Table I provides measured sensor imaging characteristics.

Conclusion

The first submicron pixel image sensor is reported. Characterization results show promising performance. While dark current is comparable to that of 3T CMOS APS image sensors, it is higher than that of state-of-the-art 4T CMOS APS. This is due to the storage and transfer of charge along the Si/SiO_2 interface. Lower dark current may be achievable using channel and stop implants. While the crosstalk is acceptable at short wavelengths, process modifications such as the addition of a graded epi region may help to improve it at long wavelengths.

Acknowledgments

The authors thank CH Tseng, David Yen, Chun-Yao Ko, JC Liu, Ming Li, and SG Wu from the CIS R&D group at TSMC for fabrication. Keith is supported by a Hertz Foundation Fellowship.

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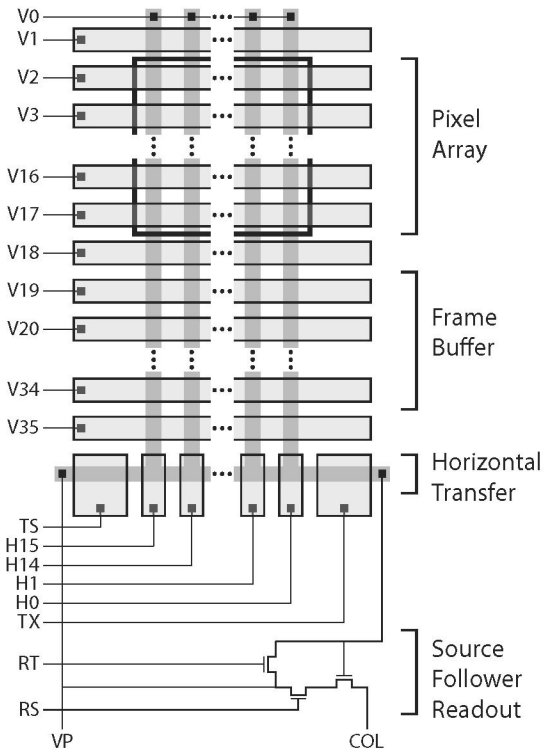

Fig. 1. FFT-CCD image sensor schematic. Actual test structure size is 16 × 16.

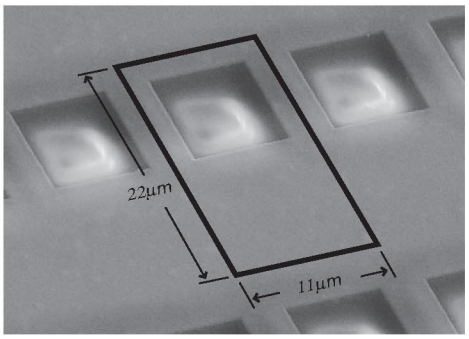

Fig. 2. A view of the fabricated test structures showing the metal opening on top of the 16 × 16 image sensor active area.

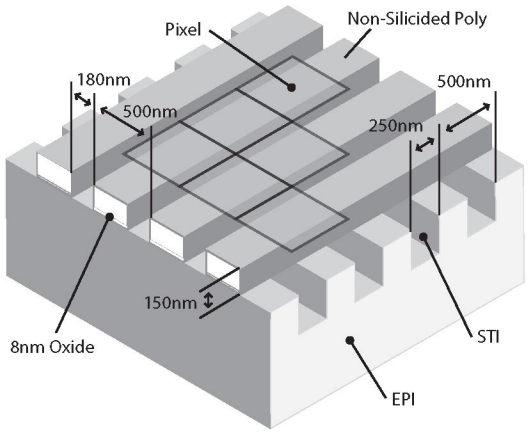

Fig. 3. A view of a 4×4 portion of the pixel array showing pattern-doped poly and STI channel stops and critical device dimensions.

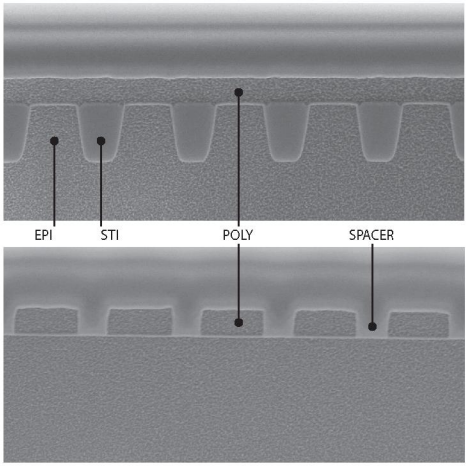

Fig. 4. SEM cross-section into channel (top), and along channel (bottom).

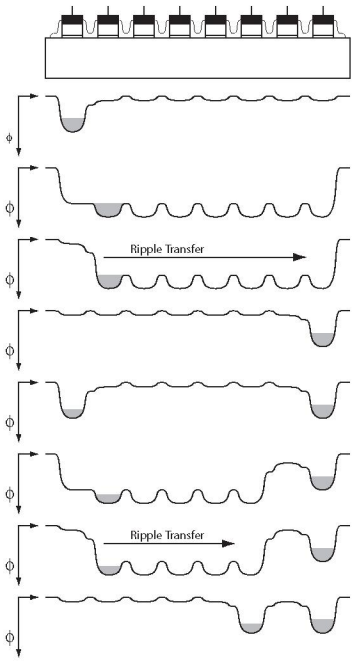

Fig. 5. Illustration of ripple charge transfer, which is used for both horizontal and vertical readout. Charge stored at every other electrode is shown here.

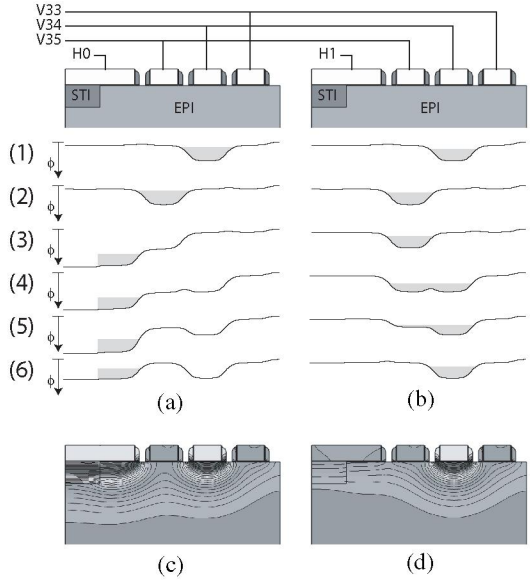

Fig. 6. Details of the vertical to horizontal transfer. (a) Transfer from row 34, column 0 to H0. (b) Effect on charge at column 1. (c) Final potential profile for column 0. (d) Final potential profile for column 1.

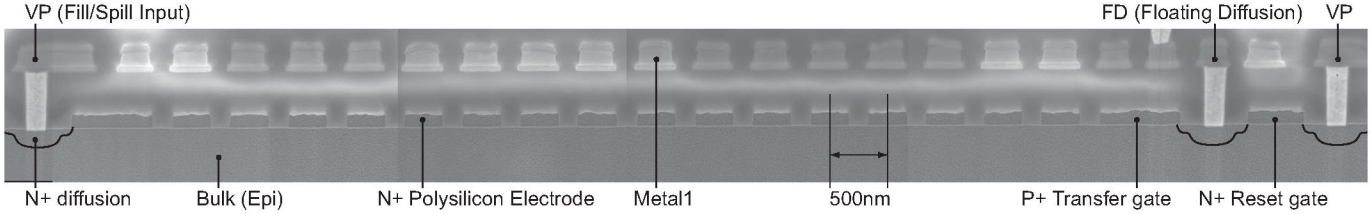

Fig. 7. SEM of full 16-stage horizontal CCD showing fill/spill input for electrical testing, floating diffusion for output charge to voltage conversion, and the reset gate.

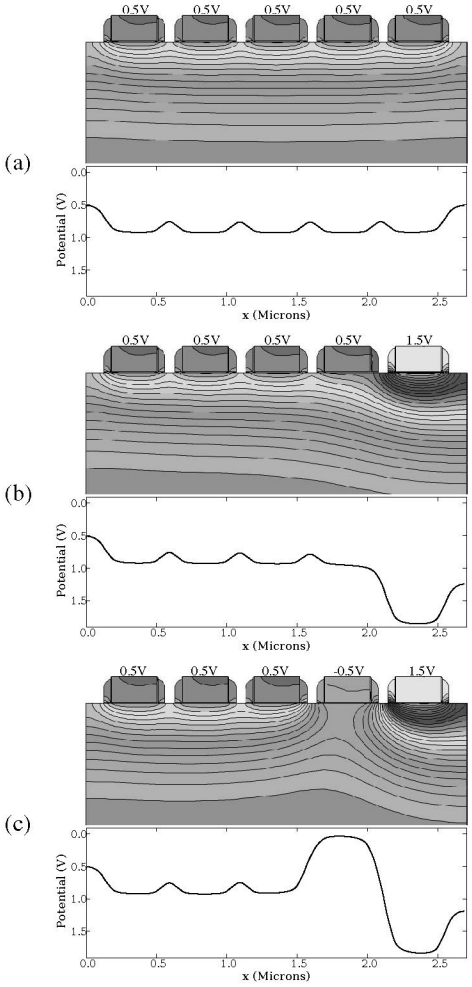

Fig. 8. Simulations of surface potential using electrode voltages V_{store} = 0.5V, V_{transfer} = 1.5V, and V_{isolate} = -0.5V. Plot (a) shows the barrier potentials between electrodes with bias V_{store}. Plot (b) shows the removal of the barrier with bias V_{transfer}. Plot (c) shows the isolation condition using V_{isolate}.

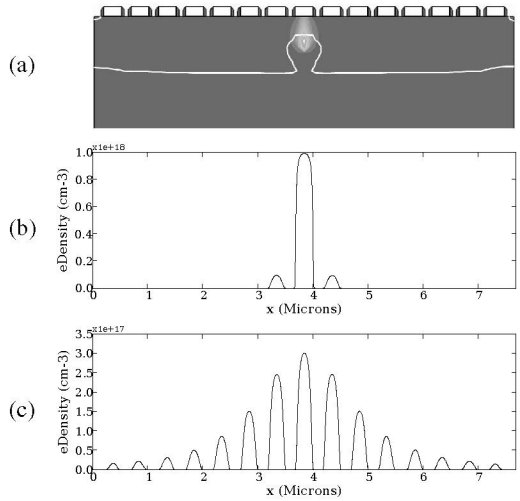

Fig. 9. Simulation of 500e-h pairs induced in the bulk at various depths. (a) Initial charge density shown for depth of 0.5 μm. After 50ns, the electron density is measured under each electrode. (b) Distribution for 0.5μm depth. (c) Distribution for 2.0μm depth.

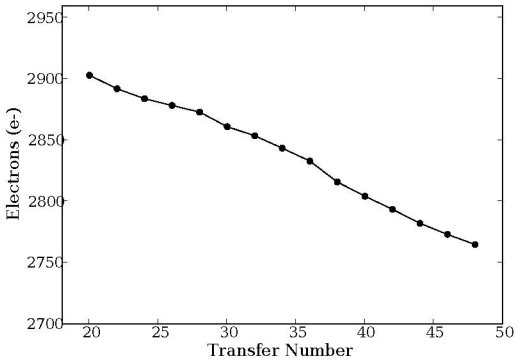

Fig. 10. Measured electrons versus the number of transfers for 3000e- packets. The slope over the small range shows CTE of 99.9%.

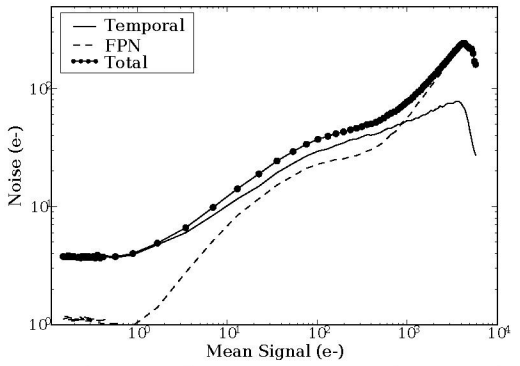

Fig. 11. Photon transfer curve at 1/30 second exposure showing read noise of 3.7e- and PRNU limitation at high illumination.

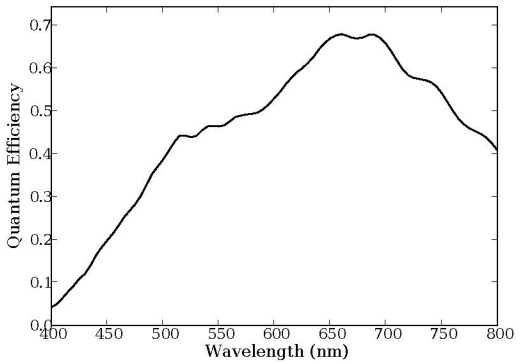

Fig. 12. Measured QE at 5nm intervals showing strongest response at 650nm. The response in the blue region is reasonable due to the 65% poly coverage of the active pixel area.

Parameter	Value	Remarks
Well capacity	3550e-	Interlaced
Conversion Gain	193μV/e-	
Responsivity	480e-/lux-s	At 550nm
Read Noise	3.7e- rms	
Dark Current	50e-/sec	3.22nA/cm^2
DSNU	25%	
PRNU	5.8%	
Dynamic Range	60dB	961:1
Peak SNR	28dB	25:1

Table I. Measured sensor characteristics at room temperature.